

FIG. 1

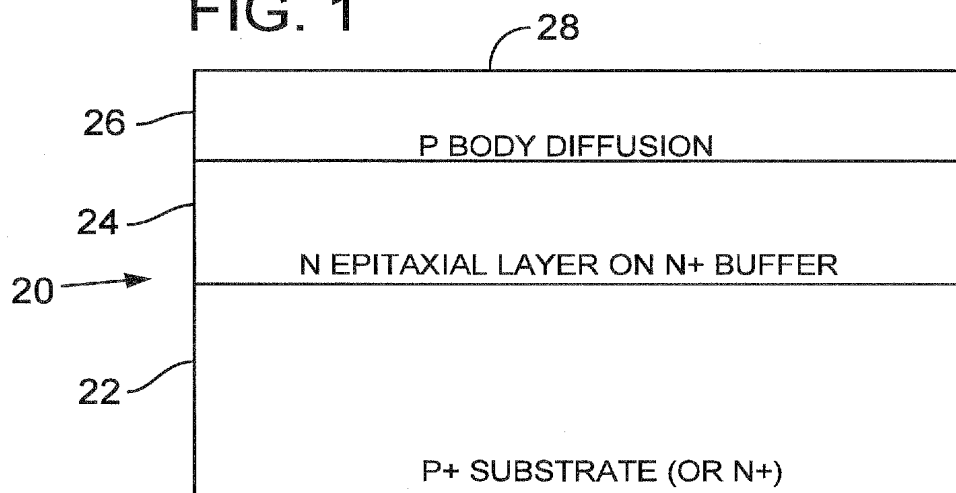
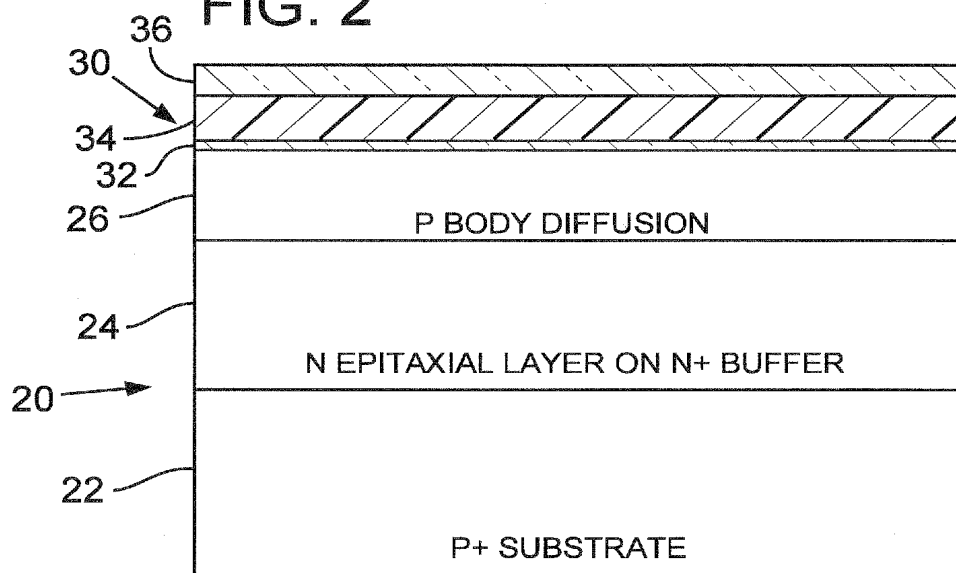
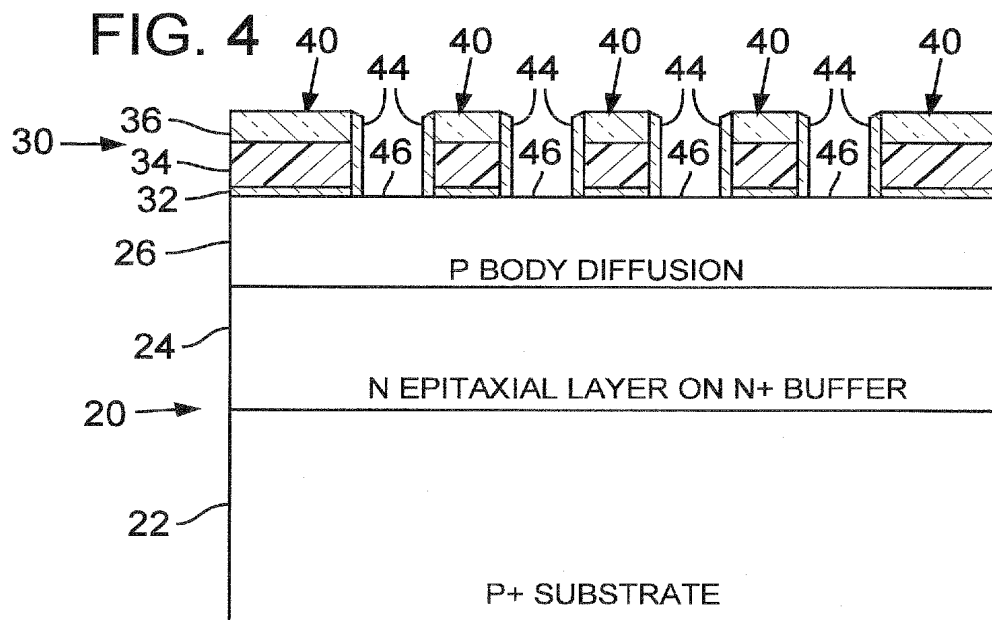
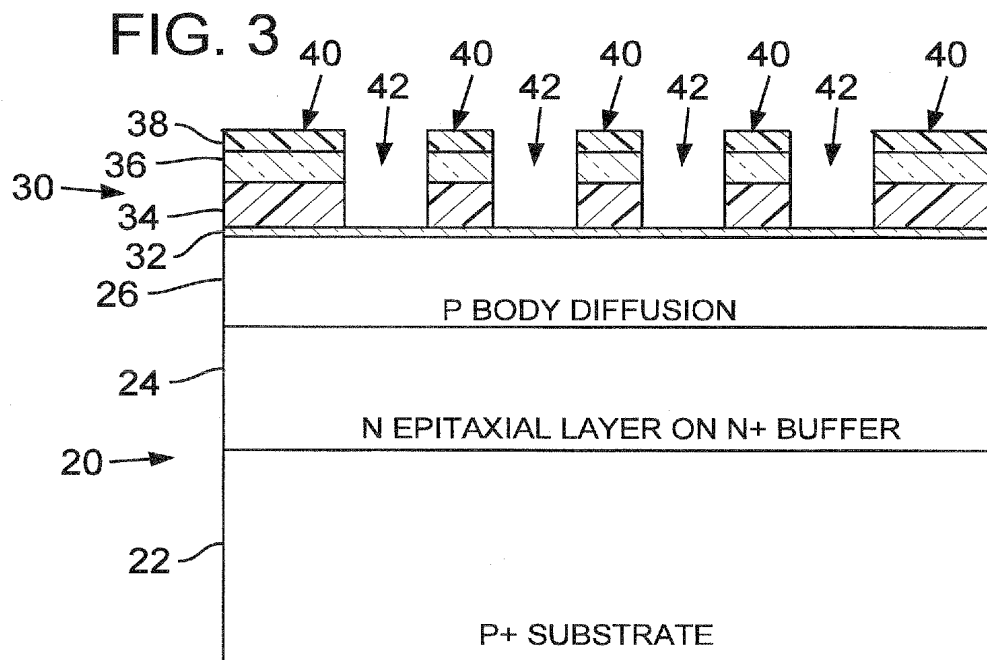


FIG. 2





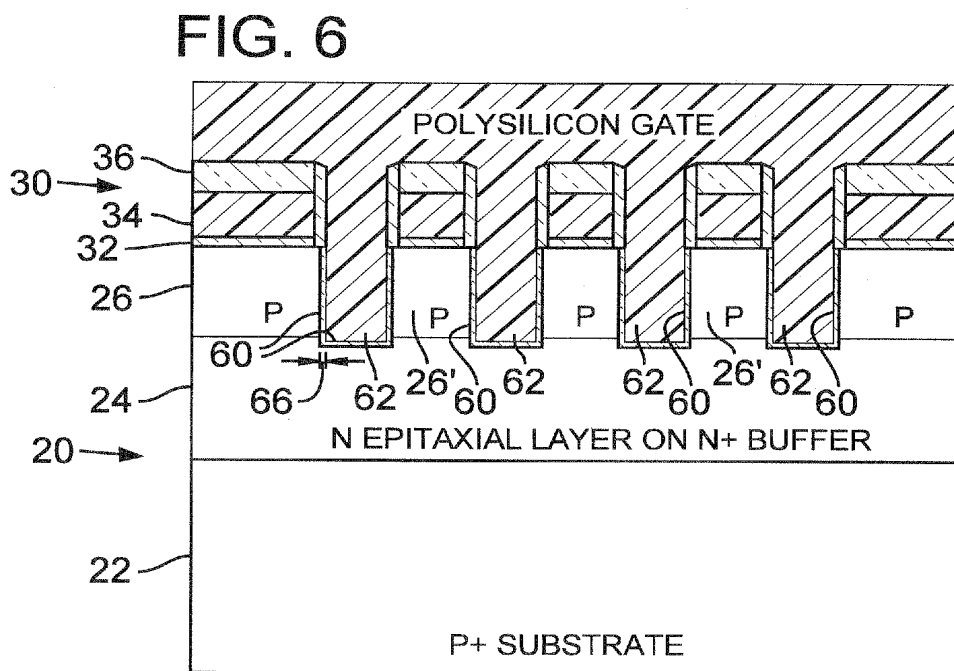
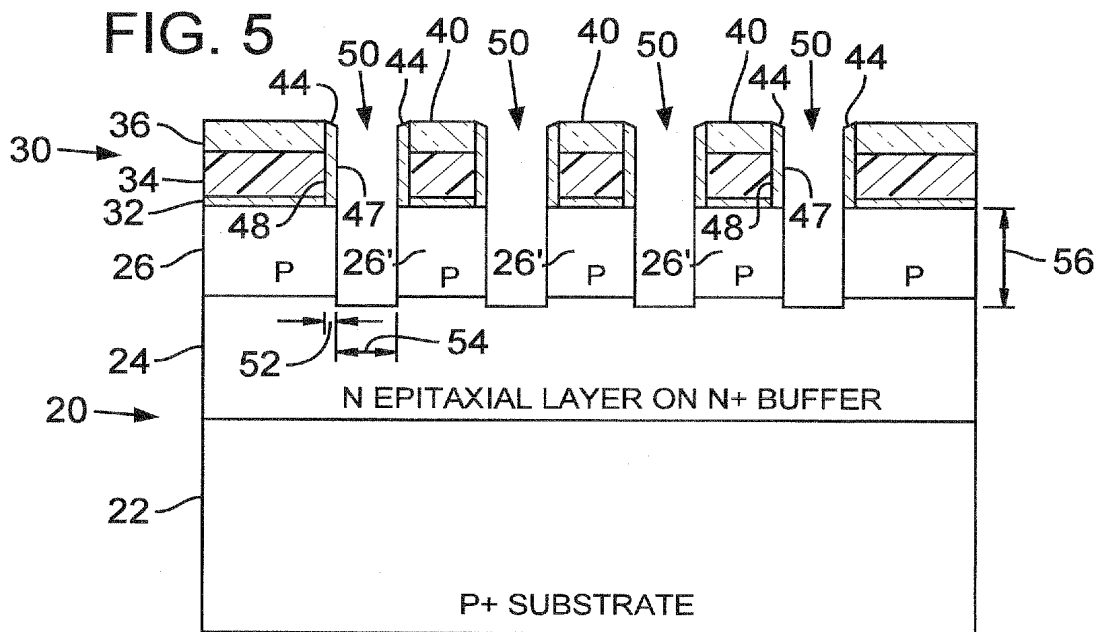


FIG. 6B

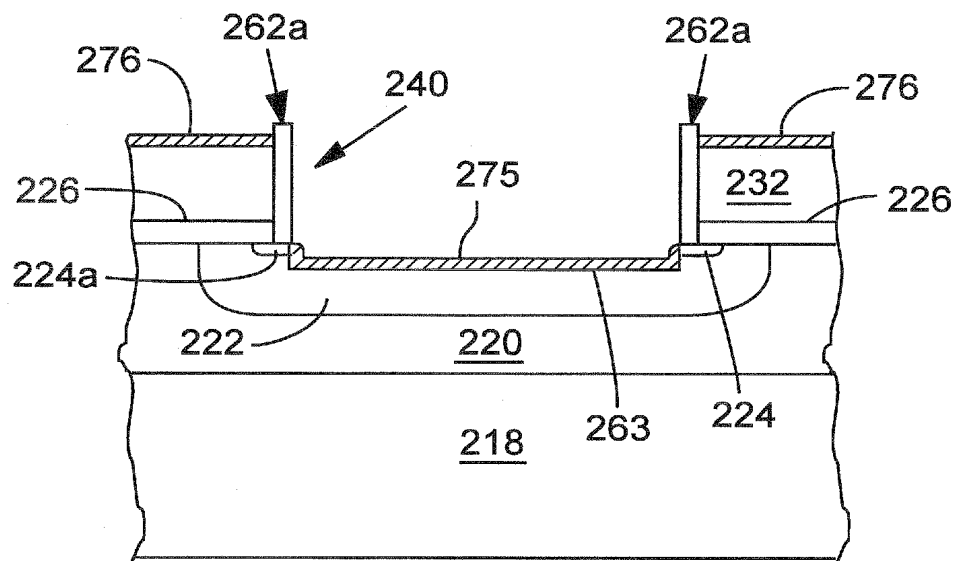


FIG. 6C

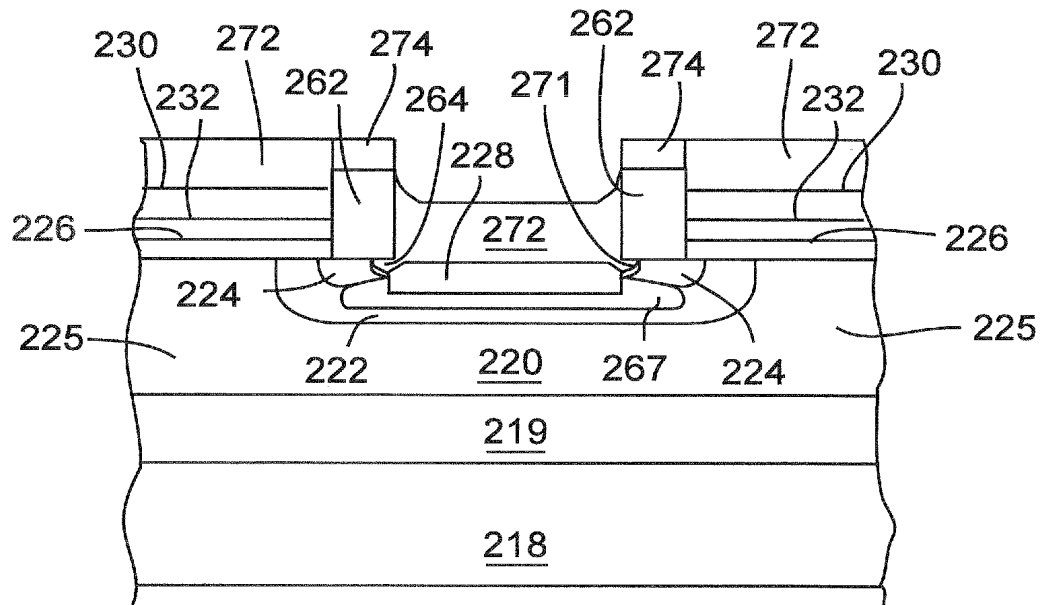


FIG. 7

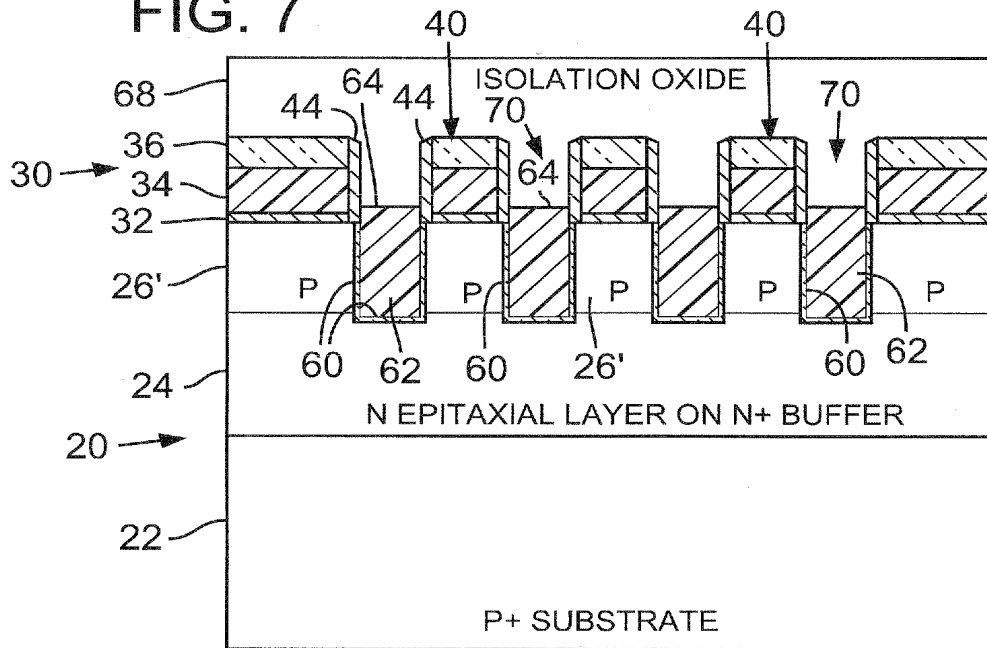


FIG. 8

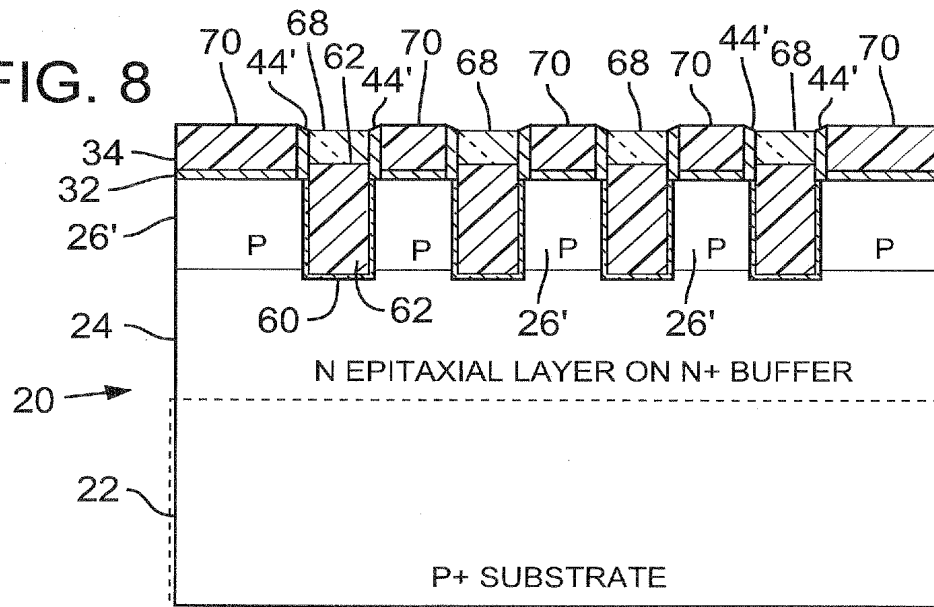


FIG. 9

A cross-sectional view of a semiconductor device. The structure consists of a P+ substrate (22) and an N EPITAXIAL LAYER ON N+ BUFFER (20). Within the N epitaxial layer, there are four P regions (26) separated by N regions (26'). Each P region (26) contains a vertical structure (44') with a central core (62) and an outer shell (60). The top surface of the P regions is labeled 28', and the top surface of the N regions is labeled 28'. The side walls of the P regions are labeled 48, and the side walls of the N regions are labeled 48'. The top surface of the P+ substrate is labeled 24. The top surface of the N epitaxial layer is labeled 26. The top surface of the P regions is labeled 68.

FIG. 10

The diagram shows a cross-sectional view of a semiconductor device. At the bottom is a **P+ SUBSTRATE**. Above it is an **N EPITAXIAL LAYER ON N+ BUFFER**. The structure consists of a series of alternating regions. From left to right, there is an **N+** region (labeled 28'), followed by a **P** region (labeled 26'). This is followed by a series of four identical repeating units. Each unit consists of a **P** region (labeled 60) with a **62** feature inside, and an **N+** region (labeled 72) on top. The **N+** regions are separated by **P** regions (labeled 72). The top surface of the **N+** regions is labeled 44', and the top surface of the **P** regions is labeled 68. The left side of the device is labeled 20, 22, 24, and 26'.

FIG. 11 is a cross-sectional view of a semiconductor device. The device is built on a P+ substrate (22). An N epitaxial layer on an N+ buffer (20) is grown on the substrate. A series of N+ regions (60, 62, 68, 80, 86, 90) are formed in the N epitaxial layer, separated by P regions (24, 26''). The N+ regions are doped with N+ ions, and the P regions are doped with P ions. A gate stack (44', 48) is formed on top of the N+ regions. The gate stack consists of a gate oxide layer (44') and a gate electrode (48). The source/drain region (82, 84) is formed in the N+ regions, and the gate oxide layer (44') is formed on top of the source/drain region. The gate oxide layer (44') is formed on top of the N+ regions, and the gate electrode (48) is formed on top of the gate oxide layer. The source/drain region (82, 84) is formed in the N+ regions, and the gate oxide layer (44') is formed on top of the source/drain region. The gate oxide layer (44') is formed on top of the N+ regions, and the gate electrode (48) is formed on top of the gate oxide layer. The source/drain region (82, 84) is formed in the N+ regions, and the gate oxide layer (44') is formed on top of the source/drain region. The gate oxide layer (44') is formed on top of the N+ regions, and the gate electrode (48) is formed on top of the gate oxide layer.

FRONTSIDE METALLIZATION

94

N+

26"

P

60

62

96

68

44

86

90

24

20

N EPITAXIAL LAYER ON N+ BUFFER

22

P+ SUBSTRATE

98

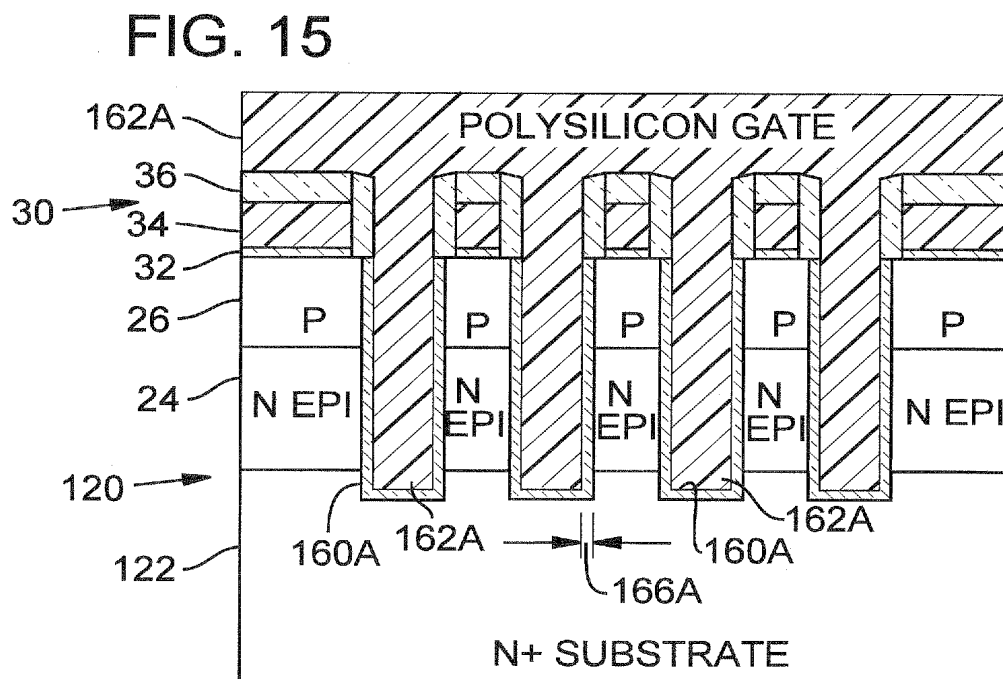
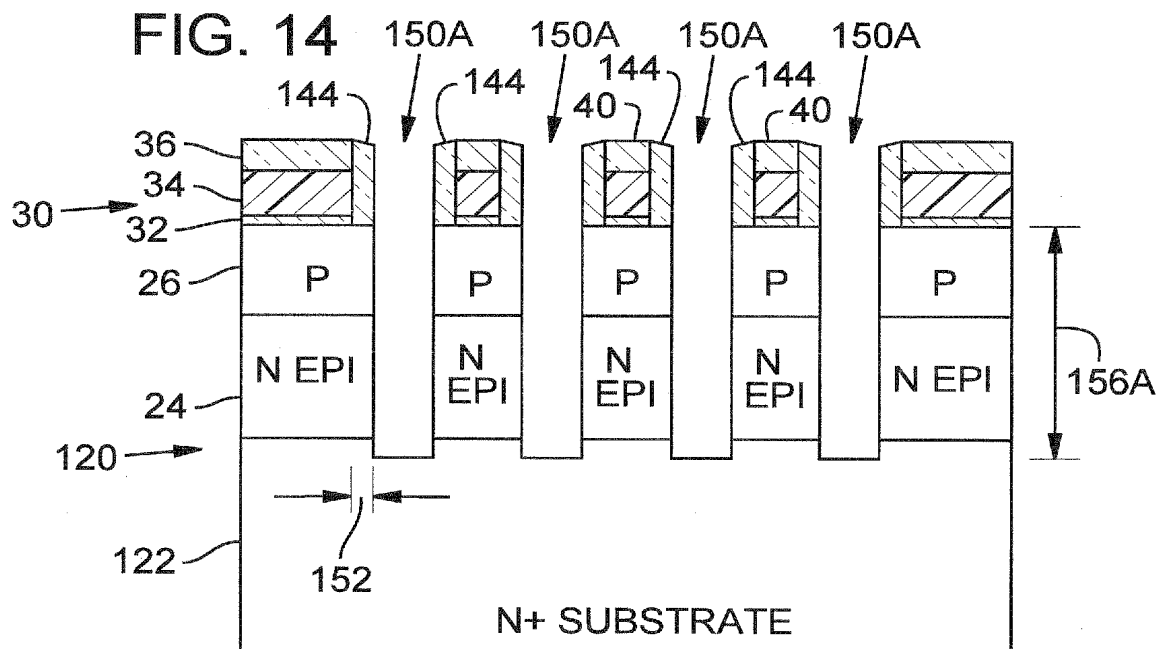


FIG. 16

150B 144 150B 144 150B 150B

36 30 34 32 26 P 24 N EPI 120 122 160A 162A 156B

N+ SUBSTRATE

[illegible]

FIG. 18

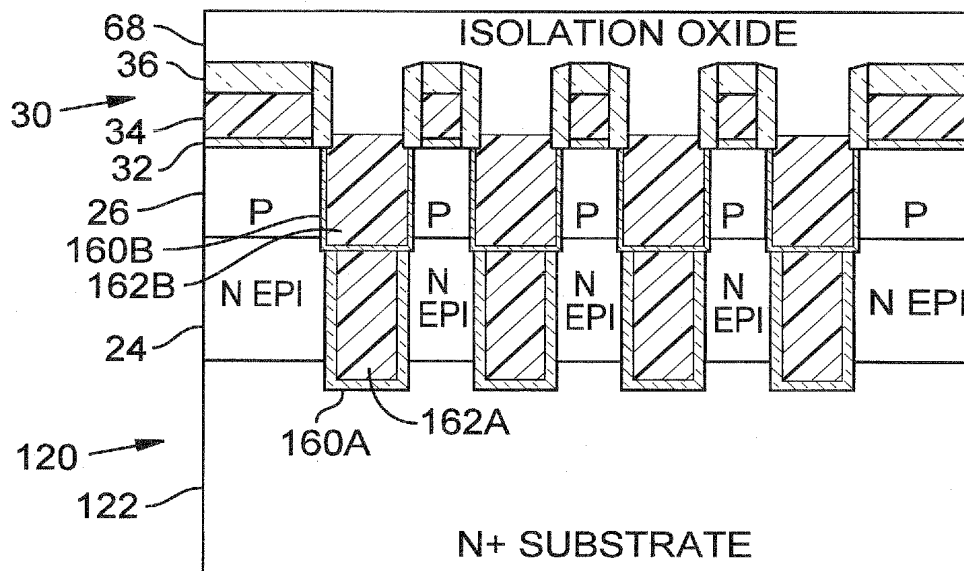


FIG. 19

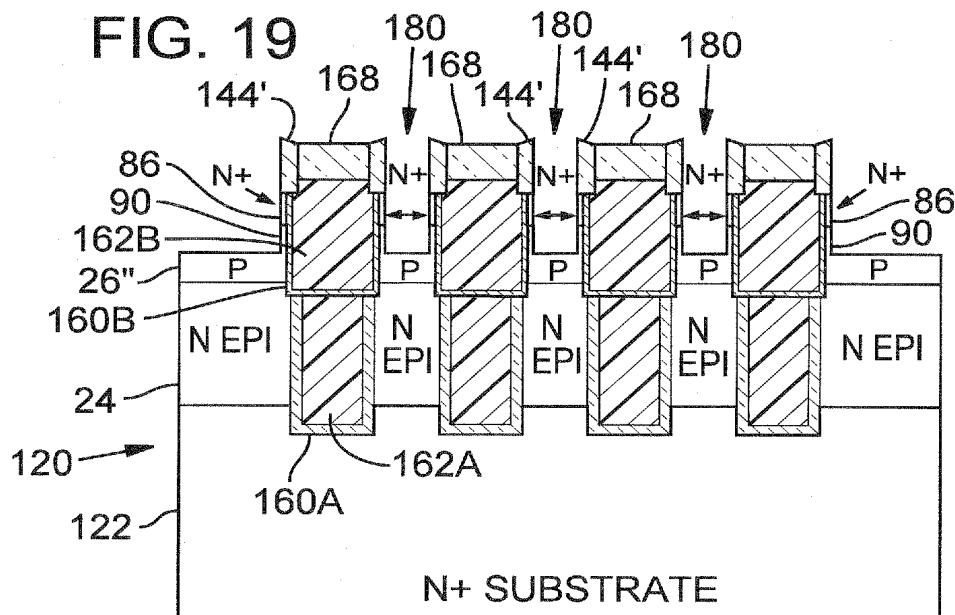


FIG. 20

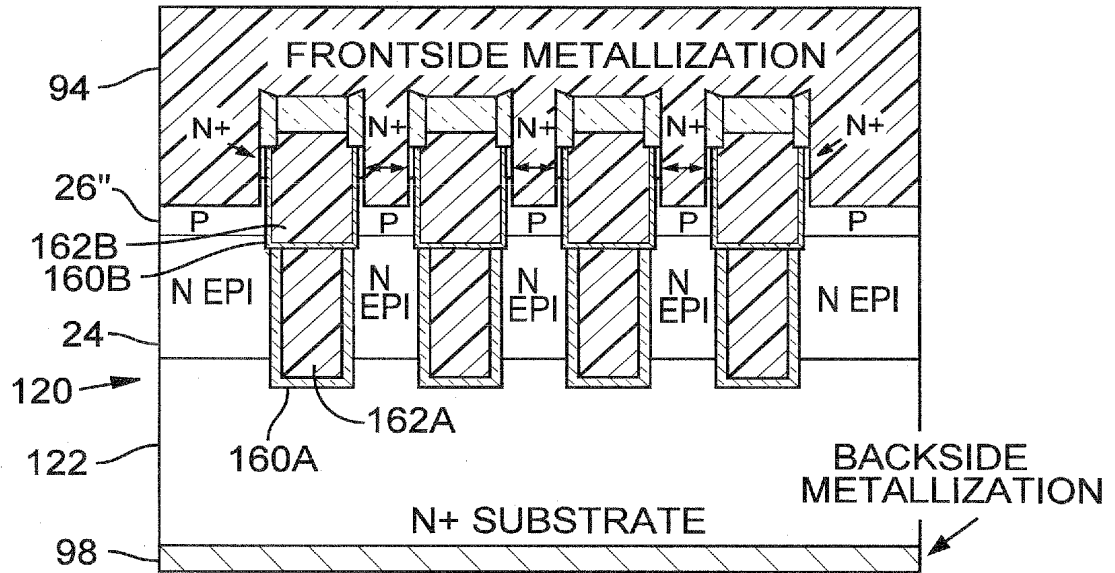


FIG. 21

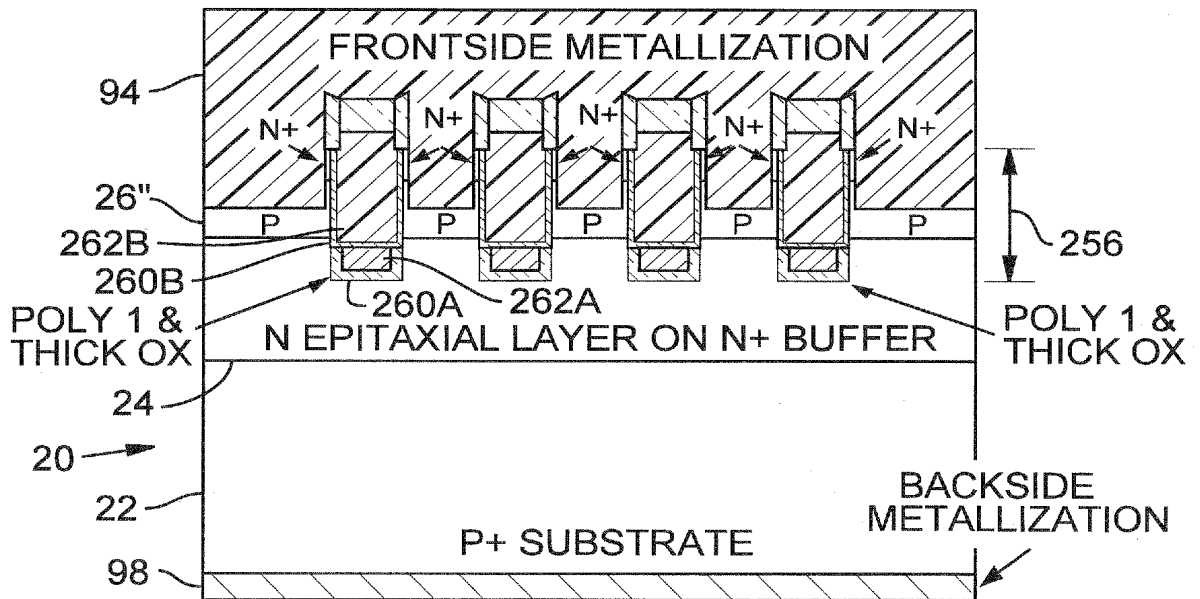


FIG. 22

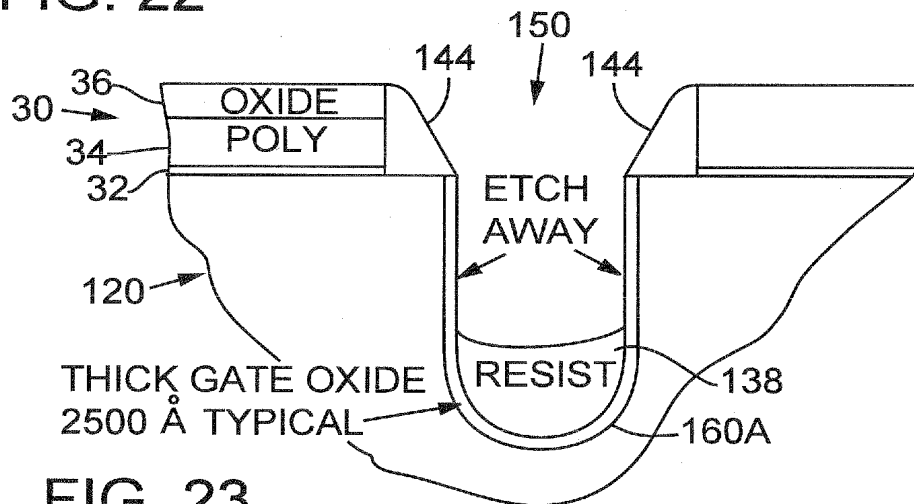


FIG. 23

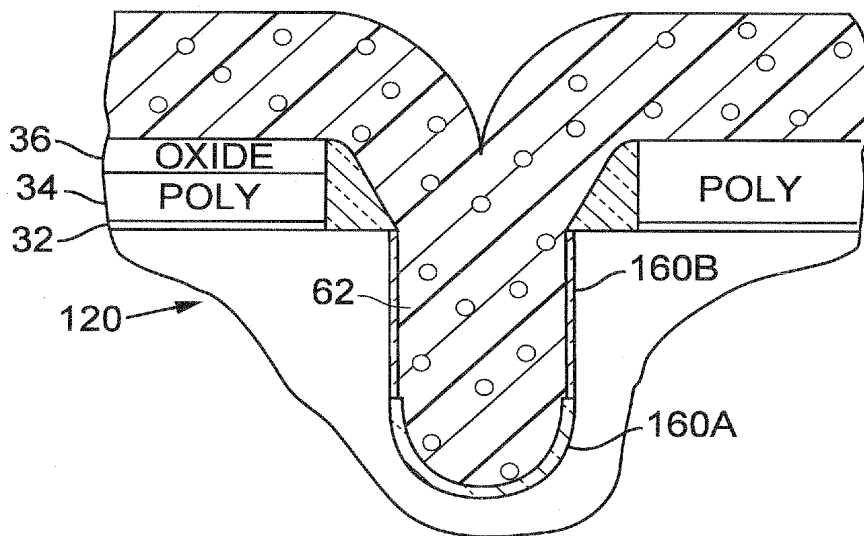


FIG. 24

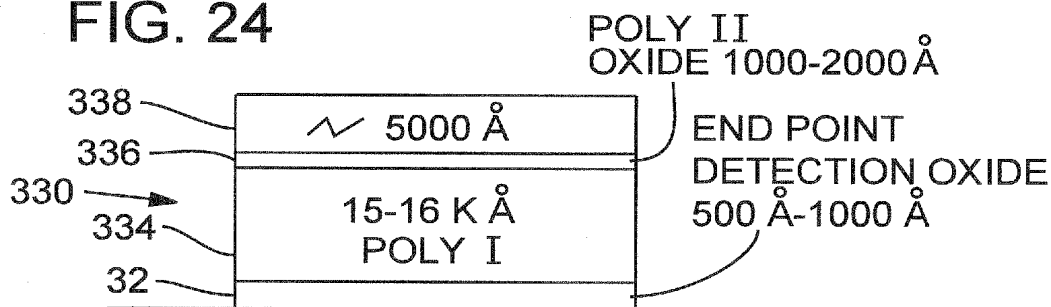
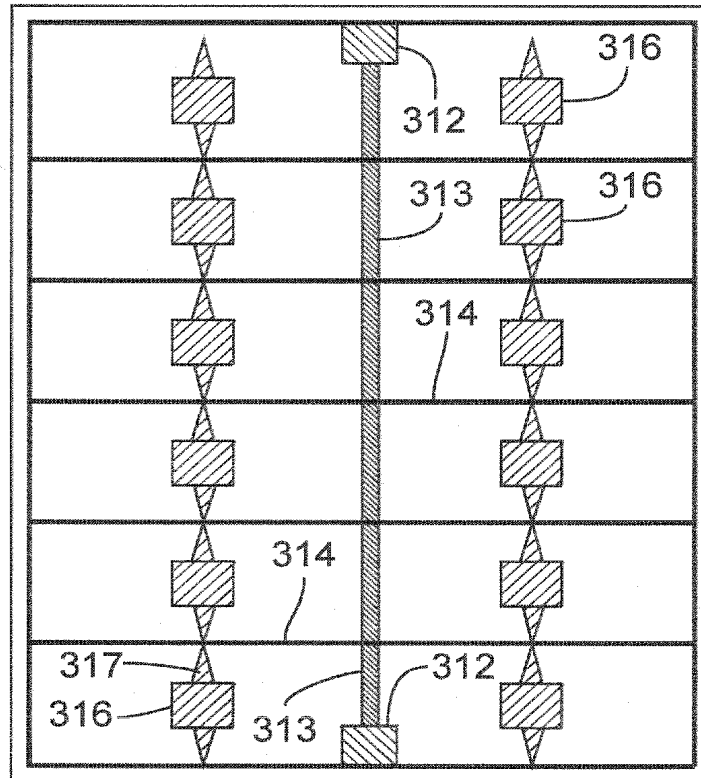






FIG. 25



- | | | | |
|---|---------------------------------|---|-------------------------|
|  | 60 X 25 MIL
SOURCE PAD |  | 25 X 35 MIL
GATE PAD |
|  | MAIN GATE
BUS 4MIL WIDE | | |
|  | SECONDARY GATE
BUS 2MIL WIDE | | |